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REMARKS

This application has been carefully reviewed in light of the Office Action dated May 24, 2007. Claims 1 to 4 and 7 to 9 are pending in the application. Claim 1, the sole independent claim, has been amended. Reconsideration and further examination are respectfully requested.

Applicant wishes to thank the Examiner for the courtesies and thoughtful treatment accorded Applicant's representative during the April 30, 2007 and May 1, 2007 telephonic interviews. During those interviews, the Applicant's representative requested that a new Office Action be mailed, since the §§ 102 and 103 rejections entered in the March 23, 2007 Office Action were not seen to treat the language of the amended claims. The Examiner agreed, and issued the instant Office Action, which is dated May 24, 2007.

Claims 1 to 4 and 7 to 9 were rejected under 35 U.S.C. § 112, first paragraph, for alleged failure to provide written description support for Claim 1.

Claim 1 has been amended to recite that "an issuance of a request for using the processor bus from one of the built-in processor and the external bus interface to which the asserted enable signal is input can be suppressed and the other one of the built-in processor and the external bus interface can use the processor bus exclusively". This is seen to be described at least at page 6, lines 7 to 27 of the specification. Reconsideration and withdrawal are therefore respectfully requested.

Claims 1 to 3 and 7 to 9 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 6,347,294 (Booker); and Claim 4 was rejected under 35 U.S.C. § 103(a) over

Booker in view of U.S. Patent No. 6,041,400 (Ozcelik). Reconsideration and withdrawal are respectfully requested.

The present invention generally concerns a processor system on a single semiconductor substrate, wherein the processor system is provided with a built-in processor, a memory controller, an external bus interface that can connect an external processor from outside of a single semiconductor substrate, a processor bus which is connected with the built-in processor and the external bus interface, and a connection unit that mutually connects the memory controller and the processor bus. First and second signal lines for inputting first and second enable signals are connected to reset signal lines of the built-in processor and the external bus interface, respectively. In addition, one of the first and second enable signals is asserted while the other one of the first and second enable signals is deasserted, so that an issuance of a request for using the processor bus from one of the built-in processor and the external bus interface to which the asserted enable signal is input can be suppressed and the other one of the built-in processor and the external bus interface can use the processor bus exclusively.

Thus, among its many features, the present invention provides that (i) a processor bus is connected with a built-in processor and an external bus interface, (ii) first and second signal lines for inputting first and second enable signals are connected to reset signal lines of the built-in processor and the external bus interface, respectively, and (iii) one of the first and second enable signals is asserted while the other one of the first and second enable signals is deasserted, so that an issuance of a request for using the processor bus from one of the built-in processor and the external bus interface to which the asserted

enable signal is input can be suppressed and the other one of the built-in processor and the external bus interface can use the processor bus exclusively. The applied references of Booker and Ozcelik are not seen to disclose or suggest at least these features.

As understood by Applicant, Booker discloses that an EXCPU 14 and an EMCPU 26 obtain common access to a DCRX logic 160. The EXCPU 14 gains control of DCRX logic 160 or memory interface through arbitration. See Booker, column 5, line 57 to column 6, line 5; and Figure 4.

However, Booker is not seen to disclose or suggest that EXCPU 14 and EMCPU 26 connect to a same bus, muchless that EXCPU 14 and EMCPU 26 use such a same bus exclusively. Morevoer, Booker is not seen to disclose or suggest that one of the EXCPU 14 and EMCPU 26 is asserted, while the other is deasserted.

Accordingly, Booker is not seen to disclose or suggest that (i) a processor bus is connected with a built-in processor and an external bus interface, (ii) first and second signal lines for inputting first and second enable signals are connected to reset signal lines of the built-in processor and the external bus interface, respectively, and (iii) one of the first and second enable signals is asserted while the other one of the first and second enable signals is deasserted, so that an issuance of a request for using the processor bus from one of the built-in processor and the external bus interface to which the asserted enable signal is input can be suppressed and the other one of the built-in processor and the external bus interface can use the processor bus exclusively.

In addition, Ozcelik has been reviewed and is not seen to compensate for the deficiencies of Booker.

Accordingly, based on the foregoing amendments and remarks, independent Claim 1 as amended is believed to be allowable over the applied references.

The other claims in the application are each dependent from the independent claims and are believed to be allowable over the applied references for at least the same reasons. Because each dependent claim is deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

No other matters being raised, it is believed that the entire application is fully in condition for allowance, and such action is courteously solicited.

Applicant's undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

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